Abstract

GENERATING A LOCK SIGNAL INDICATING WHETHER AN OUTPUT CLOCK SIGNAL GENERATED BY A PLL IS IN LOCK WITH AN INPUT REFERENCE SIGNAL

A PLL lock generator using one circuit (lock detection block) to indicate whether an output clock signal is locked to an input reference signal, and another circuit to determine whether the signals are out-of-lock. A lock generation blocks examines several indications of lock detection before generating a lock signal. Short term fluctuations (such as jitter) in lock and out-of-lock indications may be ignored. An embodiment of lock detection block contains a first flip-flop latching an up signal and clocked by a down signal, and a second flip-flip latching the down signal and clocked by an up signal. The up and down signals may be generated by a phase frequency detector. An examination circuit examines the output of lock detection block to generate the lock indications.

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